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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,825	03/31/2000	David L Black	07072-100001	2354

22494 7590 10/03/2002

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EXAMINER
LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/540,825	BLACK ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2, 3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

a) Page 10, line 19, the reference sign "electrical cabinet 300" is not in Fig. 3 and 4.

b) Page 10, lines 19-20, the reference sign "eight front-end director boards 190_1-190_8" is not in Fig. 3 and 4.

c) Page 10, lines 21-22, the reference sign "back-end directors 200_1-200_{32}" is not in Fig. 3 and 4.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On page 6, line 20, the term "ports-123_{32}" should be substituted by --ports 123_1-123_{32}--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walton et al. [US 6,389,494 B1; hereinafter Walton] in view of Gilbertson et al. [US 6,178,466 B1; hereinafter Gilbertson].

Referring to claims 1 and 8, Walton discloses a data storage system (computer system 100 of Fig. 2) for transferring data (See col. 7, lines 13-15) between a host computer/server (host computer 112 of

Fig. 2) and a bank of disk drives (disk drive bank 116 of Fig. 2) through a system interface (interface 118 of Fig. 2), such system interface comprising: (a) a plurality of first director boards (front-end director 0-3 $122_{0\text{-}3}$ of Fig. 2) coupled to host computer/server; each one of said first director boards having: (i) a plurality of first directors (bus interfaces between CPU and To/From Host Computer 112 in Fig. 4); and (ii) a crossbar switch (X bar switch 123 of Fig. 4) having input/output ports coupled to said first directors on such one of said first director boards and a pair of output/input ports (See the connection between X bar switch and bus interface in Fig. 4); (b) a plurality of second director boards (rear-end director 4-7 $122_{4\text{-}7}$ of Fig. 2) coupled to said bank of disk drives (disk drive bank 116 of Fig. 2), each one of said second director boards having: (i) a plurality of second directors (bus interfaces between CPU and To/From Disk Drive Bank in Fig. 5); and (ii) a crossbar switch (X bar switch 123 of Fig. 5) having input/output ports coupled to said second directors on such one of said second director boards and a pair of output/input ports (See the connection between X bar switch and bus interface in Fig. 5); (c) a data transfer section (coupling node and memory region A-D in Fig. 3 as combined) having a cache memory (memory region A-D in Fig. 3), such cache memory being coupled to said plurality of first and second directors (See col. 5, lines 32-55); (d) a message network (cache memory 0 120_0 and cache memory 1 120_1 in Fig. 2 as combined) comprising: a pair of message network boards (cache memory 0 120_0 and cache memory 1 120_1 in Fig. 2), each one of such message network boards having: a switching network (control logic section ASICs in Fig. 3) having a plurality input/output ports ($P_{0\text{-}7}$ in Fig. 3), each one of such pair of input/output ports being coupled to a corresponding one of said pair of output/input ports of said crossbar switches of said plurality of first director boards and said plurality of second director boards (See Fig. 2-5); and (e) wherein said first and second directors control data transfer between said host computer and said bank of disk drives in response to messages passing between said first directors and said second directors through said message network to facilitate said data transfer between host computer/server and said bank of disk drives (See col. 2, line 59 through col. 3, line 5) with such data

passing through said cache memory (i.e., memory region A-D in Fig. 3) in said data transfer section (i.e., coupling node and memory region A-D in Fig. 3 as combined).

Walton does not disclose said message network is operative independently of said data transfer section.

Gilbertson discloses a memory storage unit (MSU in Fig 2) in a symmetrical multiprocessor system (Fig. 1), wherein a message network (Address/function Interface 220 and Memory Controller 250 in Fig. 2 as combined) is operative independently of a data transfer section (Data Interface 210 and Memory Data Crossbar 230 in Fig. 2 as combined). Refer to col. 6, lines 15-32.

Walton and Gilbertson are analogous art because they are from a similar problem solving area, viz., system interface.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said independent operation method between message network (i.e., Address/function Interface and Memory Controller as combined) and said data transfer section (i.e., Data Interface and Memory Data Crossbar as combined), as disclosed by Gilbertson, to said data message network board (i.e., cache memory) which is not independently operating with said data transfer section (i.e., coupling node and memory regions as combined), as disclosed by Walton, for the advantage of providing a method of maximizing bandpass on said data transfer interface (See col. 24, lines 26-27; Gilbertson).

6. Claims 2-6 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walton [US 6,389,494 B1] in view of Gilbertson [US 6,178,466 B1] as applied to claims 1 and 8 above, and further in view of Sne et al [US 5,890,207; hereinafter Sne].

Referring to claims 2 and 9, Walton, as modified by Gilbertson, discloses all the limitations of claims 2 and 9 including a controller (bus interface which is between CPU and To/From BUS D in Fig. 4; Walton) for transferring said messages (i.e., interface state data; Walton) between said message network

(i.e., cache memory 0-1 120_0-120_1 in Fig. 2 as combined; Walton) and such one of said first directors (i.e., front-end director 0-3 122_{0-3} of Fig. 2; Walton) except that does not teach a data pipe in said first director. Sne discloses a high performance integrated cached storage device, wherein a first director (i.e., front end SCSI Director in Fig. 3A) includes: a data pipe (i.e., SCSI pipe in Fig. 3A) coupled between an input of such said first director (See col. 17, lines 1-3) and a cache memory (i.e., global memory in Fig. 3A). Refer to col. 17, lines 1-7.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data pipe, as disclosed by Sne, in said first director, as disclosed by Walton in view of Gilbertson, for the advantage of being able to add greater depth by incorporating a prefetch mechanism that permits write data to be put out to buffers or transceivers at the backend awaiting bus access, while up to two full 32 word buffers of assembled memory data is stored in dual port ram, and memory data words are assembled in the pipeline gate arrays for passing to the dual port ram buffers (See col. 5, lines 33-61 of Sne).

Referring to claims 4 and 11, Walton, as modified by Gilbertson, discloses all the limitations of claims 3 and 10 including a controller (bus interface which is between CPU and To/From BUS D in Fig. 5; Walton) for transferring said messages (i.e., interface state data; Walton) between said message network (i.e., cache memory 0-1 120_0-120_1 in Fig. 2 as combined; Walton) and such one of said second directors (i.e., rear-end director 4-7 122_{4-7} of Fig. 2; Walton) except that does not teach a data pipe and a controller in said second director.

Sne discloses a high performance integrated cached storage device, wherein a second director (i.e., back end SCSI Director in Fig. 3E) includes: a data pipe (i.e., SCSI pipe in Fig. 3E) coupled between an input of such said second director (See col. 18, lines 43-46) and a cache memory (i.e., global memory in Fig. 3E). Refer to col. 18, lines 41-46.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data pipe, as disclosed by Sne, in said first director, as disclosed by Walton in view of Gilbertson, for the advantage of being able to add greater depth by incorporating a prefetch mechanism that permits write data to be put out to buffers or transceivers at the backend awaiting bus access, while up to two full 32 word buffers of assembled memory data is stored in dual port ram, and memory data words are assembled in the pipeline gate arrays for passing to the dual port ram buffers (See col. 5, lines 33-61 of Sne).

Referring to claims 3 and 10, these claims 3 and 10 are exactly same as the claims 4 and 11. Therefore, the rejection of the claims 4 and 11 is applied to the rejection of these claims 3 and 10.

Referring to claims 5 and 12, Walton, as modified by Gilbertson, discloses all the limitations of claims 5 and 12 including a microprocessor (CPU in Fig. 4; Walton) a controller (bus interface which is between CPU and To/From BUS D in Fig. 4; Walton) for transferring said messages (i.e., interface state data; Walton) between said message network (i.e., cache memory 0-1 120_0-120_1 in Fig. 2 as combined; Walton) and such one of said first directors (i.e., front-end director 0-3 $122_{0\text{-}3}$ of Fig. 2; Walton) except that does not teach a data pipe and a controller in said first director.

Sne discloses a high performance integrated cached storage device, wherein a first director (i.e., front end SCSI Director in Fig. 3A) includes: a data pipe (i.e., SCSI pipe in Fig. 3A) coupled between an input of such said first director (See col. 17, lines 1-3) and a cache memory (i.e., global memory in Fig. 3A). Refer to col. 17, lines 1-7.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data pipe, as disclosed by Sne, in said first director, as disclosed by Walton in view of Gilbertson, for the advantage of being able to add greater depth by incorporating a prefetch mechanism that permits write data to be put out to buffers or transceivers at the backend awaiting bus access, while up to two full 32 word buffers of assembled memory data is stored in dual port ram, and

memory data words are assembled in the pipeline gate arrays for passing to the dual port ram buffers (See col. 5, lines 33-61 of Sne).

Referring to claims 7 and 14, Walton, as modified by Gilbertson, discloses all the limitations of claims 3 and 10 including a microprocessor (CPU in Fig 5; Walton); a controller (bus interface which is between CPU and To/From BUS D in Fig. 5; Walton) for transferring said messages (i.e., interface state data; Walton) between said message network (i.e., cache memory 0-1 120_0-120_1 in Fig. 2 as combined; Walton) and such one of said second directors (i.e., rear-end director 4-7 $122_{4\text{-}7}$ of Fig. 2; Walton) except that does not teach a data pipe and a controller in said second director.

Sne discloses a high performance integrated cached storage device, wherein a second director (i.e., back end SCSI Director in Fig. 3E) includes: a data pipe (i.e., SCSI pipe in Fig. 3E) coupled between an input of such said second director (See col. 18, lines 43-46) and a cache memory (i.e., global memory in Fig. 3E). Refer to col. 18, lines 41-46.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data pipe, as disclosed by Sne, in said first director, as disclosed by Walton in view of Gilbertson, for the advantage of being able to add greater depth by incorporating a prefetch mechanism that permits write data to be put out to buffers or transceivers at the backend awaiting bus access, while up to two full 32 word buffers of assembled memory data is stored in dual port ram, and memory data words are assembled in the pipeline gate arrays for passing to the dual port ram buffers (See col. 5, lines 33-61 of Sne).

Referring to claims 6 and 13, these claims 6 and 13 are exactly same as the claims 7 and 14. Therefore, the rejection of the claims 7 and 14 is applied to the rejection of these claims 6 and 13.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mayer [US 6,009,481] discloses mass storage system using internal system-level mirroring.

MacLellan et al. [US 6,397,281 B1] disclose bus arbitration system.

Budde et al. [US 4,480,307] disclose interface for use between a memory and components of a module switching apparatus.

Cadden et al. [US 6,038,638] disclose pausing and resuming applications running in a data processing system using tape location parameters and pipes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter S. Wong can be reached on 703-305-3477. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3718 for regular communications and 703-746-9248 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2181

cel/ CEL
September 27, 2002

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER